

FIG. 1  
(PRIOR ART)

10

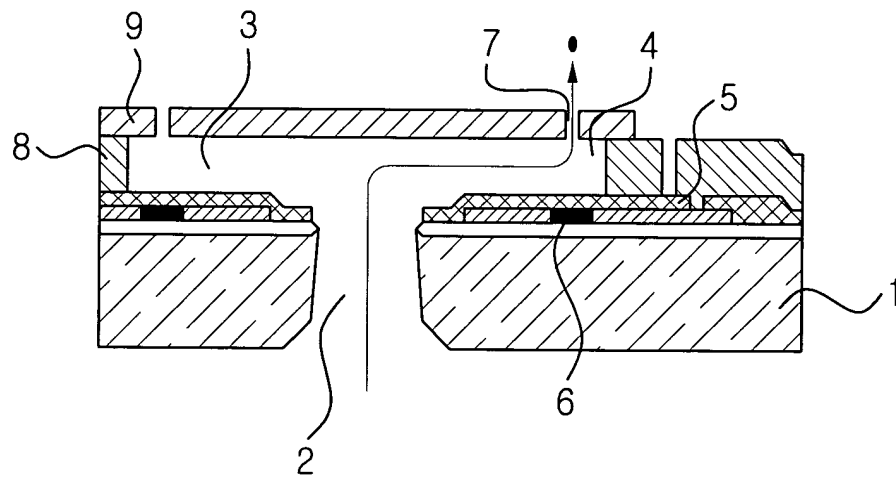


FIG. 2A  
(PRIOR ART)

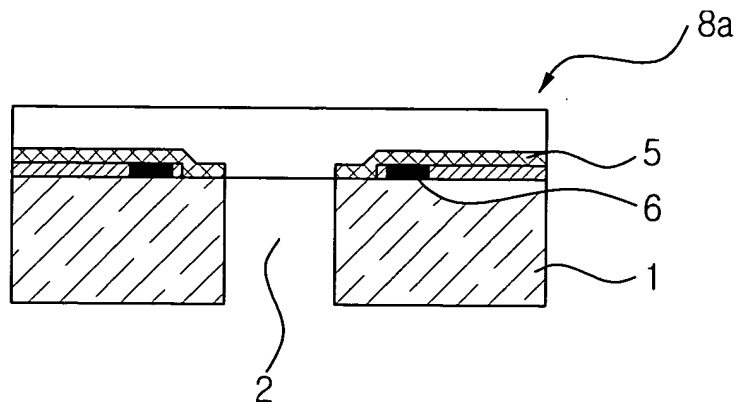


FIG.2B  
(PRIOR ART)

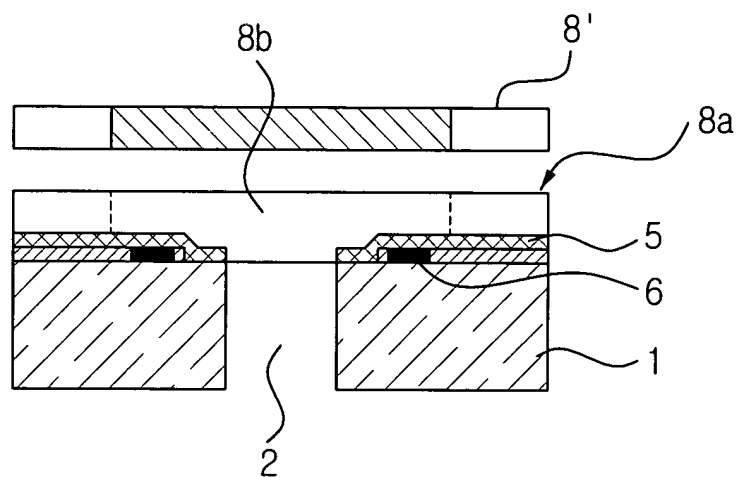
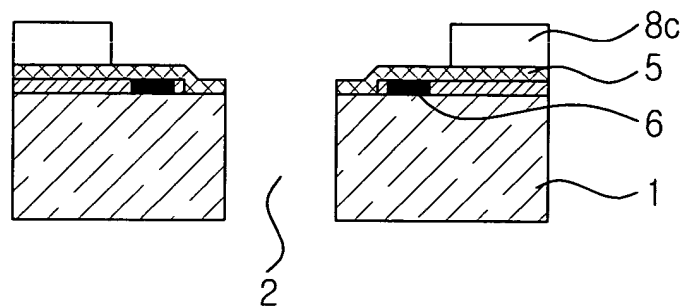


FIG.2C  
(PRIOR ART)



This diagram shows a cross-sectional view of a semiconductor device. It features two main blocks, 1 and 2, which are connected by a bridge 7. Block 1 is on the right and contains a stack of layers: a base layer 1, a layer 6, a layer 5, and a top layer 8c. A contact pad 9a is located on the top surface of block 1. Block 2 is on the left and contains a stack of layers: a base layer 3, a layer 4, and a top layer. A contact pad is also located on the top surface of block 2. The bridge 7 connects the top surfaces of blocks 1 and 2.

A cross-sectional view of a substrate 1. A thin layer 5 is formed on the top surface of the substrate 1. Two openings 6 are formed in the thin layer 5, exposing the top surface of the substrate 1.

Fig. 1 is a cross-sectional view of a semiconductor device. It shows a substrate 1 with a gate insulating layer 5 and a gate electrode 6. A gate insulating layer 8a' is formed on top of the gate electrode 6.

FIG.3C  
(PRIOR ART)

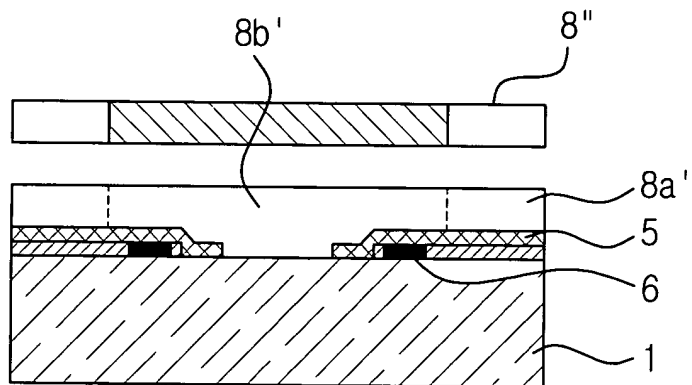


FIG.3D  
(PRIOR ART)

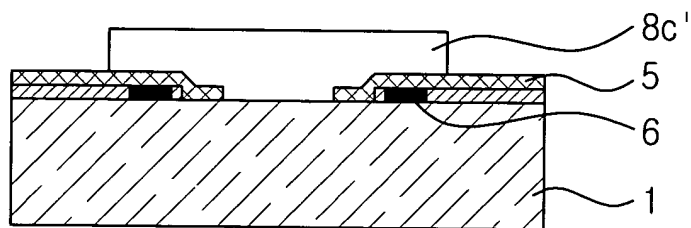


FIG.3E  
(PRIOR ART)

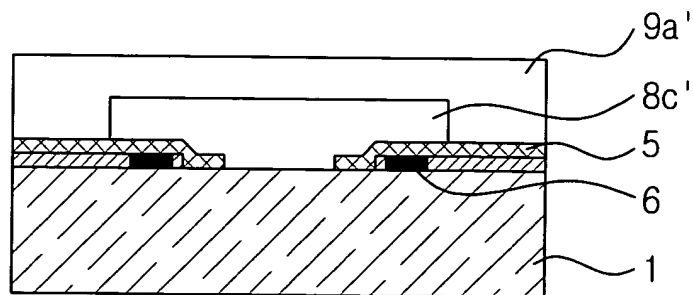


FIG.3F  
(PRIOR ART)

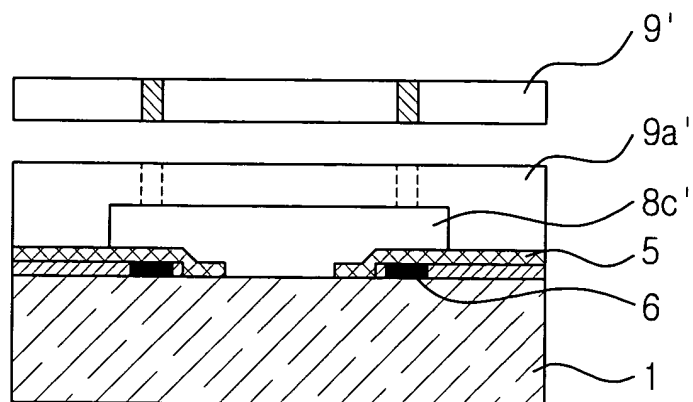


FIG.3G  
(PRIOR ART)

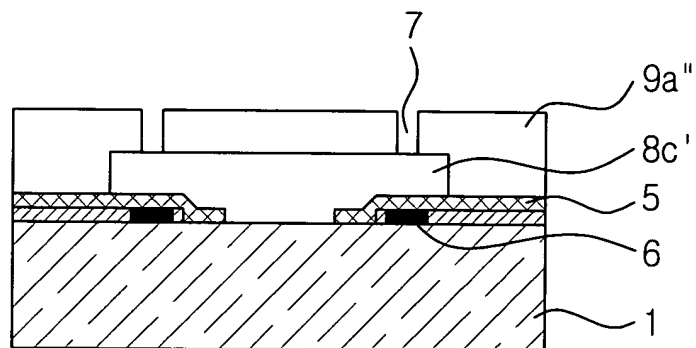


FIG.3H  
(PRIOR ART)

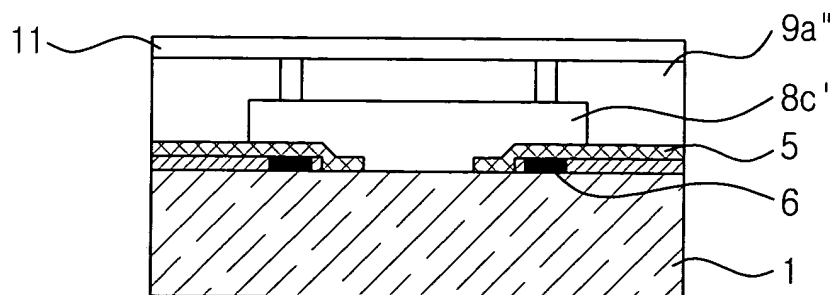


FIG.3I  
(PRIOR ART)

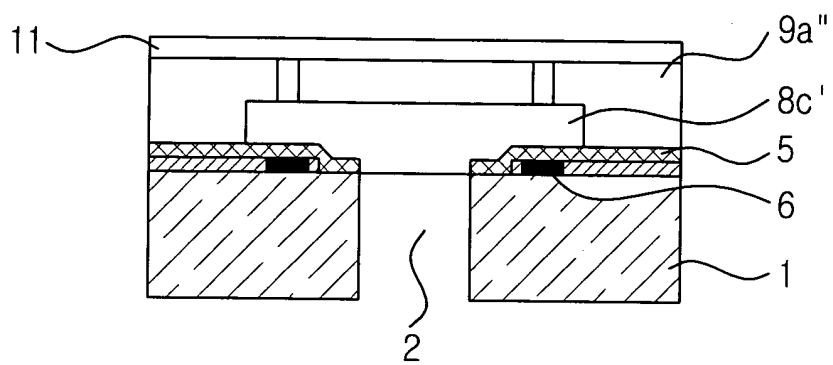


FIG.3J  
(PRIOR ART)

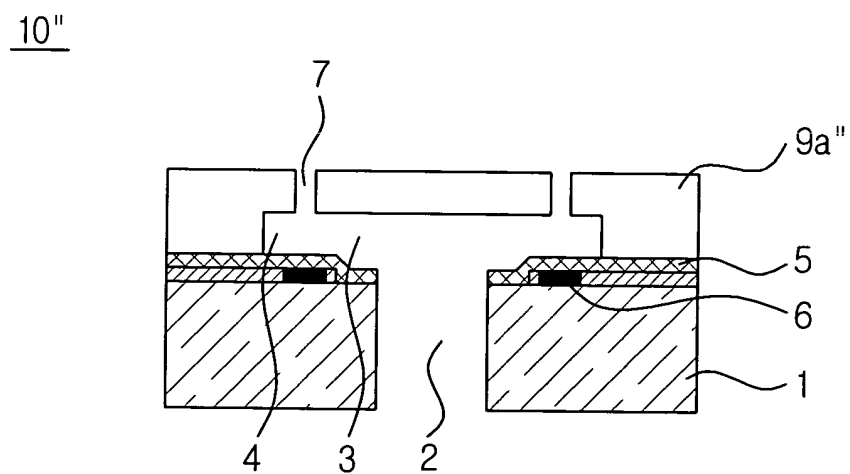


FIG.4A

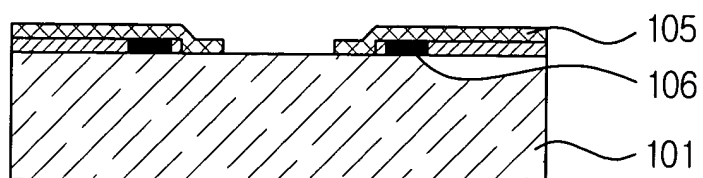
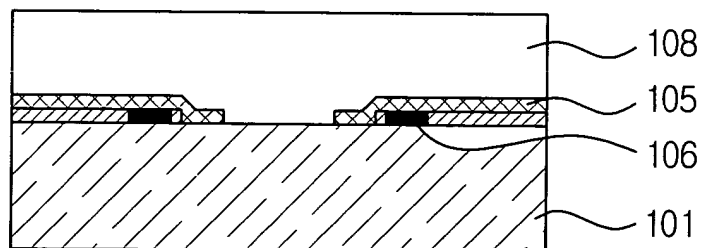
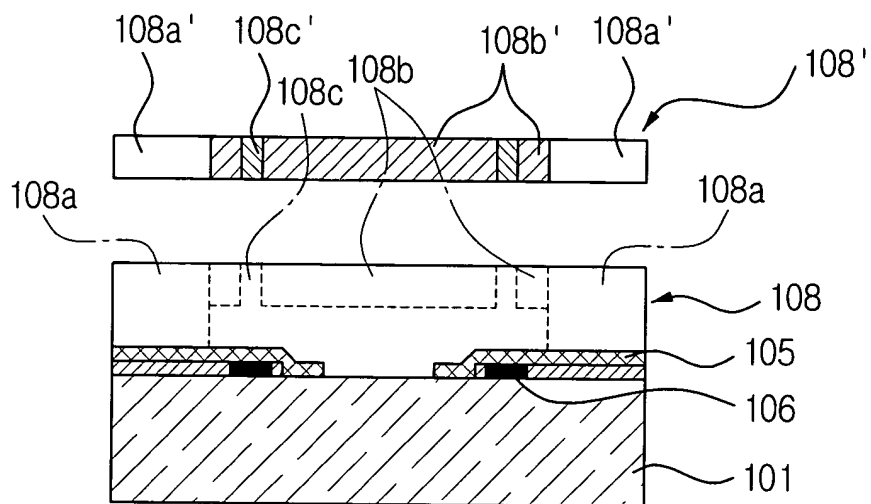


FIG.4B



# FIG. 4C



# FIG. 4D

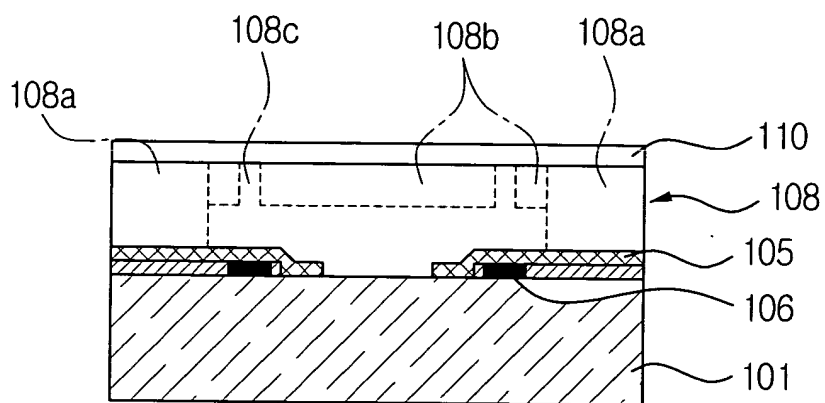




FIG.4E

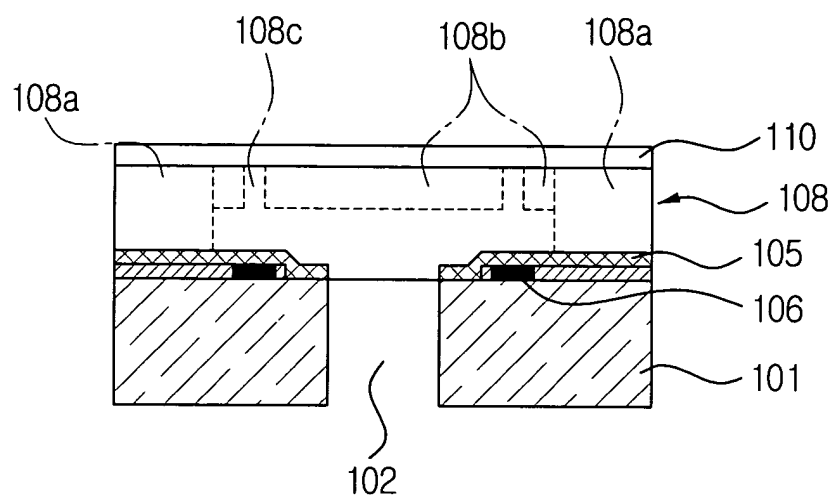
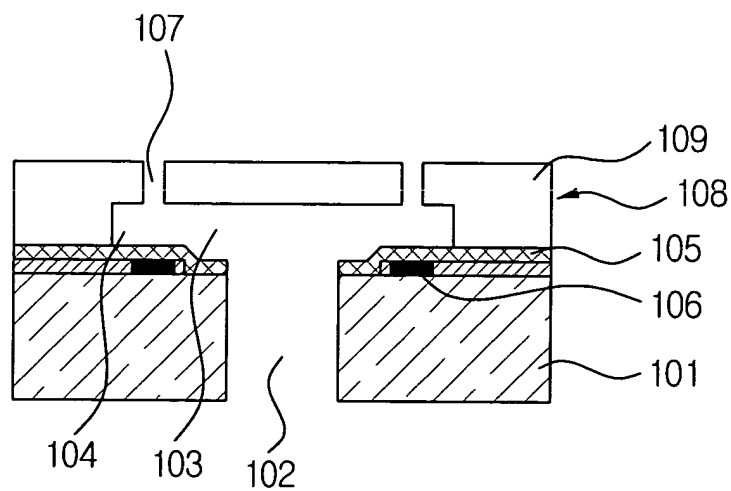
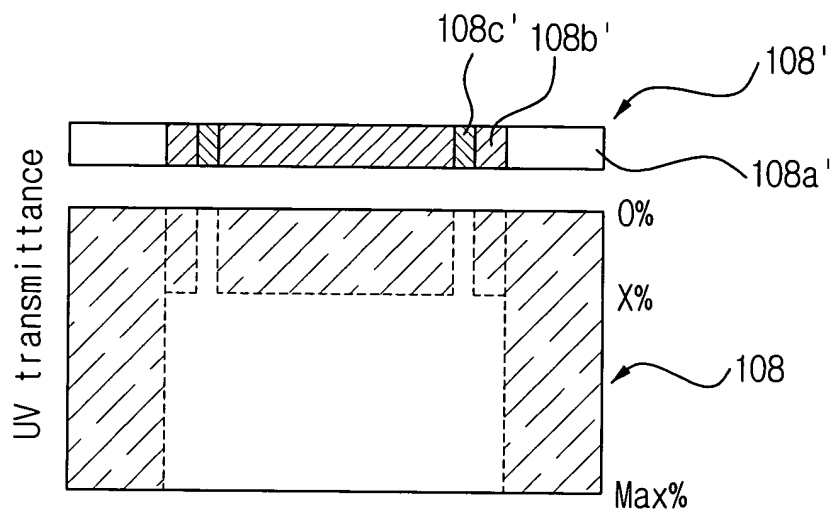


FIG.4F

100



# FIG.5A



# FIG.5B

